MULTIMEDIA UNIVERSITY

STUDENT ID NO

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# MULTIMEDIA UNIVERSITY

# FINAL EXAMINATION

**TRIMESTER 2, 2018/2019**

## ECE2046 – COMPUTER ORGANIZATION AND ARCHITECTURE

( TE/EE/CE/OPE/NANO )

9 MARCH 2019
2:30 p.m – 4:30 p.m.
( 2 Hours )

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**INSTRUCTIONS TO STUDENTS**

1. This Question paper consists of 7 pages including cover page with 5 Questions only.
2. Attempt **ALL** Questions. The distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

**Question 1**

(a) State Moore's law and discuss its consequences.

[4 marks]

(b) With the aid of a diagram, explain the Von Neumann architecture.

[6 marks]

(c) Draw a diagram showing a contemporary bus architecture used in personal computers.

[5 marks]

(d) A computer system has 1 MB of byte-addressable main memory and 8 kB of 2-way set associative cache memory. One cache line is 4 bytes.

(i) Determine the number of cache lines.

[1 mark]

(ii) Determine the size of the "tag" and "set" fields of the memory address.

[4 marks]

(iii) Figure Q1(d)(iii) shows a portion of the main memory contents (all numbers are in hexadecimal). Draw a diagram showing the cache contents after memory location ABCDE (hexadecimal) is accessed.

[5 marks]

| Address | Contents |
|---|---|
| ABCDA | 12 |
| ABCDB | 34 |
| ABCDC | 56 |
| ABCDD | 78 |
| ABCDE | 9A |
| ABCDF | BC |
| ABCE0 | DE |
| ABCE1 | F0 |

**Figure Q1(d)(iii)**

**Continued...**

**Question 2**

(a) Briefly discuss the concept of uni-programming and multi-programming.

[2 marks]

(b) List and briefly define the major types of operating system scheduling.

[3 marks]

(c) Define the term 'swapping' in the context of memory management. Explain the need of swapping mechanism.

[4 marks]

(d) A virtual memory system has a page size of 512 bytes, seven virtual pages, and four physical page frames. The page table is constructed as shown in Table Q2 (d).

Note: VPN: Virtual Page Number, and PFN: Page Frame Number.

| Virtual Page Number (VPN) | Page Frame Number (PFN) |
|---|---|
| 0 | 2 |
| 1 | 0 |
| 2 | - |
| 3 | 1 |
| 4 | 3 |
| 5 | - |
| 6 | - |

**Table: Q2 (d)**

(i) What is the difference between virtual address (i.e. logical address) and physical address?

[2 marks]

(ii) Compute the corresponding physical address of the following virtual addresses.

(I) 0

[3 marks]

(II) 2010

[3 marks]

**Continued...**

**Question 3**

(a) What are the four essential elements of a number in floating-point notation?

[1 mark]

(b) Convert C4 FC 88 00 (hexadecimal number) from IEEE single precision format to its decimal equivalent number.

[3 marks]

(c) Given $x = 0101$ and $y = 1010$ in two's complement notation (i.e., $x = 5$, $y = -6$), compute the product $p = x \times y$ using Booth's algorithm.

[7 marks]

(d) Add $26.125_{10}$ and $40.625_{10}$ using floating point arithmetic. Show how the numbers and the results would be stored using the IEEE 32-bit floating-point format.

[6 marks]

**Continued...**

**Question 4**

(a) (i) An address field in an instruction contains decimal value **500**. Identify the location for corresponding operand for the following addressing modes:

(I) Immediate addressing

[1 mark]

(II) Direct addressing

[1 mark]

(III) Indirect addressing

[2 marks]

(ii) The initial values (in decimal) in the accumulators with assembly code are given as below:

**A = 13, B = 4, C = 6, D = 5, E = 8**

**Instruction 1 (I1): MOV X, A**
**Instruction 2 (I2): ADD X, B**
**Instruction 3 (I3): MOV Y, D**
**Instruction 4 (I4): MUL Y, E**
**Instruction 5 (I5): SUB Y, C**
**Instruction 6 (I6): DIV Y, X**

(I) Determine the number of addresses of I4.

[1 mark]

(II) State TWO (2) characteristics of the addresses in I6.

[2 marks]

(III) Determine the value of accumulator X (in decimal) after I2 and before I3.

[1 mark]

(IV) Determine the value of accumulator Y (in decimal) after I4 and before I5.

[1 mark]

(V) Determine the value of accumulator Y (in decimal) after I6.

[1 mark]

(b) A control unit is made up of numerous inputs and outputs. Answer the following:

(i) Draw a block diagram of the control unit with all its inputs and outputs.

[9 marks]

(ii) List and describe the inputs.

[4 marks]

(iii) List and describe the outputs.

[2 marks]

**Continued...**

## Question 5

(a) Draw a diagram to show a 5-stage pipeline. Briefly describe each of the 5 stages.

[5 marks]

(b) State and discuss the two (2) principal reasons that have motivated CISC architecture.

[4 marks]

(c) Describe multithreading and explain how it improves computer performance.

[2 marks]

(d) Identify all dependencies that exist in the following sequence of instructions. You have to write down the instructions involved, circle the registers involved, and name the type of dependency.

```
R1 ← R4 + R2
R3 ← R1 + 1
R1 ← R4 + 1
R5 ← R3 + R4
```

[5 marks]

**End of Paper**